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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LEE, CHRISTOPHER E	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 10/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/015,076	WILLIAMS ET AL.	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5-8,13-16 and 18-21* is/are allowed.

6)☒ Claim(s) *1-4,9-12 and 17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the Amendment filed on 2nd of August 2004. Claims 1, 5-9 and 13-16 have been amended; no claim has been canceled; and claims 18-21 have been newly added since the Non-Final Office Action was mailed on 5th of May 2004. Currently, claims 1-21 are pending in this application.

Claim Rejections - 35 USC § 102

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1-4, 9-12 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Miller [US 4,780,822].

Referring to claim 1, Miller discloses a circuit (i.e., integrated circuit having semaphore circuits in the Figure) comprising: a memory element (i.e., storage elements 20, 22, 24 and 26 within the semaphore circuit 10 of the Figure) defining a semaphore allocatable to a resource (See col. 1, lines 7-10; in fact, said storage elements defining semaphore allocated to a shared memory cell); and a controller (i.e., arbiter 28 within the semaphore circuit 10 of the Figure) configured to (i) present a granted status (i.e., the signal developed on the pad 142 in the Figure) in response to a processor reading a first address (i.e., processor reading an appropriate storage element, e.g., storage element 26 within the semaphore circuit 10 of the Figure) while said semaphore has a free status (See col. 5, lines 22-58), (ii) set said semaphore to a busy status in response to said processor reading said first address while said semaphore has said free state, viz., presenting said granted status (i.e., the appropriate storage element is written in a low-logic-level, which indicates that the shared memory cell is in use; See the semaphore circuit logic within the semaphore circuit 10 of the Figure), and (iii) present said busy status in response to said processor reading said first address while said semaphore has said busy status (i.e., at once, the

appropriate storage element has set to a low-logic-level, the arbiter in the semaphore circuit logic maintains the indication, such that the shared memory cell is in use; See the semaphore circuit logic within the semaphore circuit 10 of the Figure).

Referring to claim 2, Miller teaches said controller (i.e., arbiter 28 within the semaphore circuit 10 of the Figure) is further configured to set said semaphore to said free status in response to said processor writing to said first address (See col. 5, lines 59-68; i.e., "write" (a one) into the appropriate storage element indicating that the shared memory cell is no longer in use).

Referring to claim 3, Miller teaches said controller (i.e., arbiter 28 within the semaphore circuit 10 of the Figure) is further configured to present said status of said semaphore (i.e., indicating the status of semaphore on the pad 142 in the Figure; busy: low-logic-level signal, free: high-logic-level signal) in response to said processor reading a second address (i.e., processor reading an appropriate storage element, e.g., storage element 22 in the Figure; See col. 5, lines 20-68).

Referring to claim 4, Miller teaches said controller (i.e., arbiter 28 within the semaphore circuit 10 of the Figure) is further configured to maintain said status of said semaphore (See the logic of arbiter using two NOR gates in the Figure; i.e., the logic and storage element maintains the status of semaphore) in response to said processor writing to said second address (i.e., processor sets line 114 to "write enable" and send data to the storage element 22 via line 142, and thereafter the semaphore status is maintained by said logic of arbiter according to the semaphore circuit logic in the Figure).

Referring to claim 9, Miller discloses a method of allocating a resource to a processor (See Description of the Prior Art in col. 1, lines 10+) comprising the steps of: defining a semaphore allocatable to said resource (See col. 1, lines 7-10; in fact, storage elements defining semaphore allocated to a shared memory cell); presenting a granted status (i.e., the signal developed on the pad 142 in the Figure) in response to said processor reading a first address (i.e., processor reading an appropriate storage element, e.g., storage element 26 within the semaphore circuit 10 of the Figure) while said semaphore has a free

status (See col. 5, lines 22-58); setting said semaphore to a busy status in response to said processor reading said first address while said semaphore has said free state, viz., presenting said granted status (i.e., the appropriate storage element is written in a low-logic-level, which indicates that the shared memory cell is in use; See the semaphore circuit logic within the semaphore circuit 10 of the Figure); and presenting said busy status in response to said processor reading said first address while said semaphore has said busy status (i.e., at once, the appropriate storage element has set to a low-logic-level, the arbiter in the semaphore circuit logic maintains the indication, such that the shared memory cell is in use; See the semaphore circuit logic within the semaphore circuit 10 of the Figure).

Referring to claim 10, Miller teaches the step of setting said semaphore to said free status in response to said processor writing to said first address (See col. 5, lines 59-68; i.e., "write" (a one) into the appropriate storage element indicating that the shared memory cell is no longer in use).

Referring to claim 11, Miller teaches the step of presenting said status of said semaphore (i.e., indicating the status of semaphore on the pad 142 in the Figure; busy: low-logic-level signal, free: high-logic-level signal) in response to said processor reading a second address (i.e., processor reading an appropriate storage element, e.g., storage element 22 within the semaphore circuit 10 of the Figure; See col. 5, lines 20-68).

Referring to claim 12, Miller teaches the step of maintaining said status of said semaphore (See the logic of arbiter using two NOR gates in the Figure; i.e., the logic and storage element maintains the status of semaphore) in response to said processor writing to said second address (i.e., processor sets line 114 to "write enable" and send data to the storage element 22 via line 142, and thereafter the semaphore status is maintained by said logic of arbiter according to the semaphore circuit logic within the semaphore circuit 10 of the Figure).

Referring to claim 17, Miller discloses a circuit (i.e., semaphore circuit 10 in the Figure) comprising: means for defining a semaphore (i.e., storage elements 20, 22, 24 and 26 in the Figure)

allocatable to a resource (See col. 1, lines 7-10; in fact, said storage elements defining semaphore allocated to a shared memory cell); means for presenting a granted status (i.e., means for developing the signal on the pad 142 in the Figure) in response to a processor reading a first address (i.e., processor reading an appropriate storage element, e.g., storage element 26 in the Figure) while said semaphore has a free status (See col. 5, lines 22-58); means for setting said semaphore (i.e., semaphore circuit) to a busy status in response to presenting said granted status (i.e., the appropriate storage element is written in a low-logic-level, which indicates that the shared memory cell is in use; See the semaphore circuit logic in the Figure); and means for presenting said busy status in response to said processor reading said first address while said semaphore has said busy status (i.e., at once, the appropriate storage element has set to a low-logic-level, the arbiter in the semaphore circuit logic maintains the indication, such that the shared memory cell is in use; See the semaphore circuit logic in the Figure).

Allowable Subject Matter

4. Claims 5-8, 13-16 and 18-21 are allowed.

5. The following is a statement of reasons for the indication of allowable subject matter:

The limitations of claim 5 and 13 are respectively deemed allowable over the prior art of record as the prior art fails to teach or suggest that a second memory element defining a second semaphore allocatable to said semaphore, i.e., cascaded semaphoring. The claims 6-8, 18 and 19 are the dependent claims of the said claim 5, and the claims 14-16, 20 and 21 are the dependent claims of the said claim 13.

Response to Arguments

6. Applicants' arguments filed on 2nd of August 2004 (hereinafter the Response) have been fully considered but they are not persuasive.

In response to the Applicants' argument with respect to "Miller concerns a semaphore circuit for shared memory cells. ... Miller appears to be silent regarding setting a semaphore status in response to a **read**. In particular, Miller appears to contemplate switching the status of a semaphore circuit 10 in

response to processors **writing** to registers 20 and/or 22. ..." on the Response, page 11, lines 5-16, the Examiner respectfully disagrees.

In contrary to the Applicants' statement, Miller clearly teaches setting a semaphore status in response to a processor read at col. 5, lines 32-58, such that a processor reading an appropriate storage element, e.g., storage element 26 within the semaphore circuit 10 of the Figure, and presenting a signal developed on the pad 142 in the Figure, i.e., the test number is "zero" when the resource is not in use (grant status), and it is set to "one" when the resource is in use (busy status). And, Miller further discloses that a processor is required to write a zero into the appropriate storage element before using the resource in order to initially develop a low logic level, i.e., the resource is not in use (grant status), at col. 5, lines 22-31. In other words, Miller does not contemplate switching the status of a semaphore circuit in response to processor writing to registers 20 and/or 22.

Furthermore, the Applicants fail to provide any portions of Miller to support the Applicants' allegation. Thus, the Applicants' argument on this point is not persuasive.

In response to the Applicants' argument with respect to "Claim 1 further provides a free status, a grant status and a busy status. In contrast, Miller appears to be silent regarding a free status, a grant status and a busy status, associated with the semaphore circuit 10. ..." on the Response, page 11, line 17 through page 12, line 2, the Examiner respectfully disagrees.

In contrary to the Applicants' statement, Miller clearly teaches a free status, a grant status and a busy status, such that a low logic level signal developed on a pad and generated by a processor implies the claimed subject matter "free status" because the low logic level signal allows the processor to use the resource (See col. 5, lines 20-31), a testing result indicating the processor free to use the resource implies the claimed subject matter "grant status" because the testing result "zero" shows the resource is available to be used (See col. 5, lines 49-52), and a testing result indicating the processor being in use the resource

implies the claimed subject matter "busy status" because the testing result "one" shows the resource is not available to be used (See col. 5, lines 52-55).

Thus, the Applicants' argument on this point is not persuasive.

In response to the Applicants' argument with respect to "Claim 17 provides means for setting a semaphore to a busy status in response to presenting a grant status. ... The Examiner is respectfully requested to either (i) explain how Miller discloses **setting** a busy status **in response to presenting** a granted status or (ii) withdraw the rejection." on the Response, page 12, lines 3-19, the Examiner respectfully explains how Miller discloses setting a busy status in response to presenting a granted status. Actually, the claim 17 recites the limitations "means for presenting a granted status in response to a processor reading a first address while said semaphore has a free status" and "means for setting said semaphore to a busy status in response to presenting said granted status" in lines 3-7. Therefore, it could be interpreted such as "means for setting a semaphore to a busy status in response to said processor reading a first address while said semaphore has a free status", which is clearly suggested by Miller, i.e., setting in-use state by the test result "one" (i.e., a busy status) in response to a processor reading resource while a semaphore indicates not-in-use state (i.e., a free status) by the test result "zero" (i.e., in response to presenting a granted status) at col. 5, lines 20-58.

Thus, the Applicants' argument on this point is not persuasive.

In response to the Applicants' argument with respect to "Claim 17 further provides a free status, a grant status and a busy status. In contrast, Miller appears to be silent regarding a free status, a grant status and a busy status, associated with the semaphore circuit 10. ..." on the Response, page 12, line 19 through page 12, line 2, the Examiner respectfully disagrees.

As discussed in the above argument response on the instant Office Action, page 6, line 13 through page 7, line 2, the Applicants' argument on this point is not persuasive.

In response to the Applicants' argument with respect to " Claim 3 provides a controller configured to present a status of a semaphore in response to (from claim 1) a processor reading a first address and (from claim 3) the processor reading a second address. In contrast, a mux circuit 16 of disclose only one unique address on lines 118, 122 and 124 for accessing each of the semaphore circuits 10-12. ... Therefore, Miller does not appear to disclose or suggest a controller configured to present a status of a semaphore in response to a processor reading a first address and the processor reading a second address as presently claimed. ..." on the Response, page 13, line 4 through page 14, line 5, the Examiner respectfully disagrees.

In contrary to the Applicants' statement, Miller teaches three lines 112, 124 and 126 in the Figure as a semaphore circuit addressing line (See col. 4, lines 32-37), which could address 8 different semaphore circuits, not only one address.

Furthermore, Miller teaches the arbiter within the semaphore circuit (i.e., controller) is configured to set the semaphore to the free status in response to the processor writing "one" into the appropriate storage element indicating that the shared memory cell is no longer in use (i.e., the first address; See col. 5, lines 59-68), and further the arbiter (i.e., controller) being configured to indicate the status of semaphore on the pad, i.e., busy: low-logic-level signal, free: high-logic-level signal (i.e., presenting the status of the semaphore) in response to the processor reading an appropriate another storage element, e.g., storage element 22 in the Figure (i.e., processor reading a second address; See col. 5, lines 20-68). See paragraph 3 of the instant Office Action, claims 1-4, 9-12 and 17 rejection under 35 U.S.C. 102(b) as being anticipated by Miller.

Thus, the Applicants' argument on this point is not persuasive.

Conclusion

7. Applicants' amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 571-272-3637. The examiner can normally be reached on 9:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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